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QUESTION 1

An ARM processor connected to a Generic Interrupt Controller (GIC) is handling an active interrupt 11. A new interrupt 12 that is received at the GIC is forwarded to the processor, and the active interrupt 11 is preempted. Which of the following possible values of 11's priority (P1), 12's priority (P2) and the processor's priority mask (PM) permit this to happen? Assume there are 256 priority levels implemented.

- A. P1 = 0x0F, P2 = 0x10, PM = 0xFF
- B. P1 = 0x10, P2 = 0x0F, PM = 0xFF
- C. P1 = 0x0F, P2 = 0x10, PM = 0x0
- D. P1 = 0x10, P2 = 0x0F, PM = 0x0

Correct Answer: B

QUESTION 2

Which of the following best describes the relationship between Tightly Coupled Memories (TCM), Level 1 (L1) and Level 2 (L2) cache memory systems?

- A. TCMs are a part of only L1 cache system
- B. TCMs are a part of only L2 cache system
- C. TCMs are part of both L1 and L2 cache systems
- D. TCMs are not part of either L1 or L2 cache systems

Correct Answer: D

QUESTION 3

A re-entrant interrupt handler would typically be used to:

- A. Allow an external interrupt to interrupt an SVC handler
- B. Reduce response time for higher priority interrupts
- C. Allow an interrupt handler to be relocated in memory
- D. Avoid the need for an interrupt handler to use a stack.

Correct Answer: B

QUESTION 4

Implementing loops using a decrementing counter which exits the loop when a counter reaches zero can be beneficial

for power and performance. This is because:

- A. A simpler branch instruction can be used.
- B. Decrementing variables uses less power than incrementing them.
- C. The decrement and branch operations can be encoded as a single instruction.
- D. The loop termination condition check can be integrated into the subtract operation.

Correct Answer: D

QUESTION 5

Which instruction would be used to return from a Reset exception?

- A. MOVS PC, R14
- B. MOVSPC, R13
- C. Architecturally not defined
- D. SUBS PC, R14, #4

Correct Answer: C

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