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QUESTION 1

Which ARMv7 instructions are recommended to implement a semaphore?

A. SWP, SWPB

B. TEQ, TST

C. STC, SBC

D. LDREX, STREX

Correct Answer: D

QUESTION 2

In a system using the Security Extensions, how does the Secure Monitor execute a switch from Secure to Non-secure state?

A. Encrypts Secure register contents, sets the NS bit in SCTLR and branches directly to Normal world code

B. Saves Secure register contents, sets all registers to zero, sets the NS bit in SCTLR and branches directly to Normal world code

C. Saves Secure register contents, loads Non-secure ones from memory, sets the NS bit in SCTLR and performs an exception return

D. Sets the NS bit in SCTLR and performs an exception return - all registers are banked in hardware and switched automatically

Correct Answer: C

QUESTION 3

Which of the following options lists the power modes in order of increasing overhead of entry and exit from run mode?

A. Shutdown, dormant, standby

B. Dormant, standby, shutdown

C. Shutdown, standby, dormant

D. Standby, dormant shutdown

Correct Answer: D

QUESTION 4

Which of these instructions is a correct translation of the body of function f?

```
struct T { char a; int b; };

int f(struct T *p) { return p->b; }
```

A. LDR r0, [r0], #1

B. LDR r0, [r0]. #4

C. LDR r0, [r0.#1]

D. LDR r0, [r0. #4]

Correct Answer: D

QUESTION 5

Which events would be counted using the Performance Monitoring Unit (PMU) in order to measure the data cache efficiency of an application?

A. Memory read instructions, and memory write instructions

B. Architecturally executed instructions, and instruction fetches causing a cache line refill

C. Memory access instructions causing a cache line refill, and memory read and write operations causing a cache access

D. Memory read or write operations causing a cache access, and architecturally executed instructions

Correct Answer: C