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QUESTION 1

A C code segment contains three calls to a function, foobar ().

This code segment is to be linked with a static library that defines foobar ().

Ignoring inlining, how many copies of foobar () will the ARM linker place in the output?

- A. None
- B. Always one
- C. Always three
- D. One or more depending on optimization level

Correct Answer: B

QUESTION 2

Assume a Big-Endian (BE) memory system with the following memory contents. Byte Address Contents 0x100 0x11 0x101 0x22 0x102 0x33 0x103 0x44 If R5 = 0x100, what are the contents of R4 after performing the following operation? LDR R4, [R5]

- A. 0x11223344
- B. 0x44332211
- C. 0x22114433
- D. 0x33441122

Correct Answer: A

QUESTION 3

Which one of the following debug methods is the least intrusive for analyzing a timing related bug?

- A. Place breakpoints on strategic locations to locate the problem area
- B. Instrument the code with print statements to locate the problem area
- C. Use debug hardware to place watchpoints on strategic data memory locations
- D. Use trace hardware to capture a trace log up to the point of the crash

Correct Answer: D

QUESTION 4

The following function is declared: float func(float f1, float f2);

The file file1.c contains a call to func, and is compiled with hard floating point linkage. The file file2.c contains the definition of func, and is compiled with AACPS soft floating point linkage.

Assume that the two files are successfully linked using the ARM linker and an executable is generated. The generated executable:

- A. Exhibits correct behavior, but suffers a performance penalty because the linker has to generate extra code.
- B. Exhibits correct behavior, and suffers no performance penalty.
- C. Will not execute.
- D. Exhibits incorrect behavior.

Correct Answer: D

QUESTION 5

If the memory location 0x5000 contains 0Xfff0001, what is the value of r0 after the following instructions are executed?

```
MOV r1, #0x5000
```

```
LDRSH r0, [r1]
```

```
ADD r0, r0, #1
```

(Assume a little-endian memory system)

- A. 0x00000002
- B. 0xFFFF0002
- C. 0xFFFF0001
- D. 0xFFFFFFFF

Correct Answer: A

QUESTION 6

To return from a Data Abort handler and re-execute the aborting instruction, what value should be loaded to the PC?

- A. PC=LR
- B. PC=LR44
- C. PC=LR-4
- D. PC=LR-8

Correct Answer: D

QUESTION 7

What debugger view can you use to determine which function caused an exception?

- A. The Memory view
- B. The Variables view
- C. The Call Stack view
- D. The Breakpoint view

Correct Answer: C

QUESTION 8

When a linker is removing unused sections during a static link (for example, -remove or -gc- sections), it finds the sections to keep by following all relocations starting from:

- A. The entry point(s).
- B. The function named `\\main\\`.
- C. All local functions and variables.
- D. The reset vector.

Correct Answer: A

QUESTION 9

As part of the ABI specification, the AAPCS defines which of the following?

- A. How many levels of nested function calls are permitted on ARM systems
- B. How to measure the maximum amount of stack required by an application
- C. On which mode's stack you need to save the return address in a non-leaf function
- D. Which registers need to be preserved by a function

Correct Answer: D

QUESTION 10

The following C function is compiled with hard floating point linkage.

float function(int a, float b, int c, float d);

Which register is used to pass argument c?

- A. R0
- B. R1
- C. R2
- D. R3

Correct Answer: B

QUESTION 11

When building code for both ARM and Thumb states, which tool decides for each function call whether to use a BL or BLX instruction?

- A. The linker
- B. The archiver
- C. The compiler
- D. The assembler

Correct Answer: A

QUESTION 12

When the software floating point emulation library is used, how will the parameters be passed to the following function?

```
void foo(float f1, float f2, float f3, float f4);
```

- A. On the stack
- B. In registers s0-s3
- C. In registers d0-d3
- D. In registers r0-r3

Correct Answer: D

QUESTION 13

A Programmer's View CPU model usually provides:

- A. Cycle-accurate simulation of the CPU.

- B. Instruction-accurate simulation of the CPU.
- C. Simulation of user-defined memory-mapped peripherals.
- D. Cycle-accurate simulation of the cache and memory system.

Correct Answer: B

QUESTION 14

Under which of the following circumstances is TLB maintenance always required?

- A. If a TLB miss occurs
- B. On every process switch
- C. If the TLB reports a fault
- D. When a page table entry is changed

Correct Answer: D

QUESTION 15

Which power mode describes the state where the ARM processor is powered down, but its Level 1 caches remain powered?

- A. Run mode
- B. Dormant mode
- C. Standby mode
- D. Shutdown mode

Correct Answer: B

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